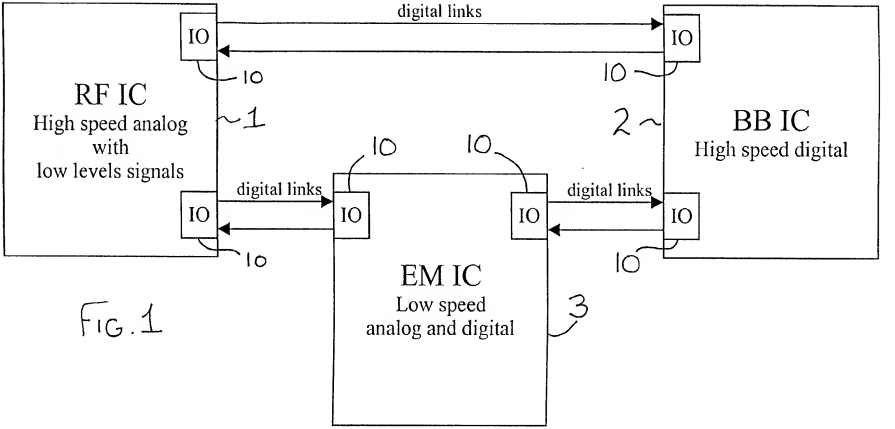


FIG. 1

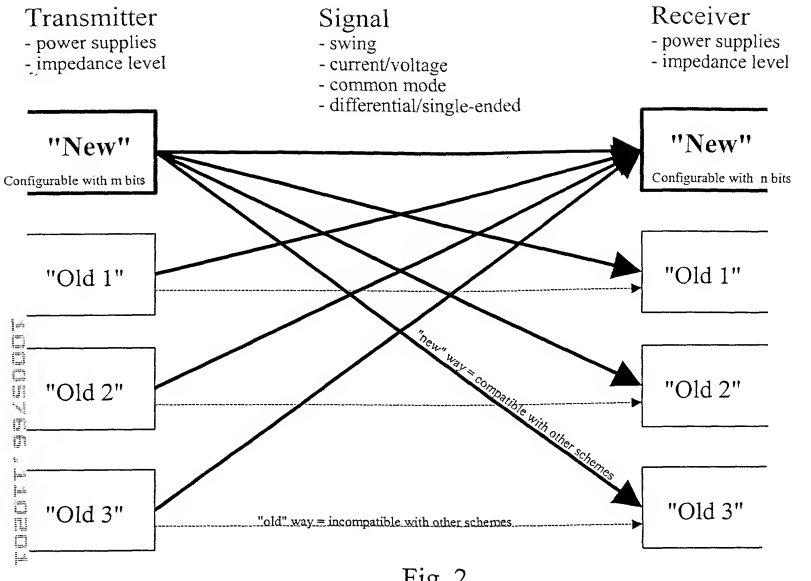

Transmitter
- power supplies
- impedance level
Signal
- swing
- current/voltage
- common mode
- differential/single-ended
Receiver
- power supplies
- impedance level
"New"
Configurable with m bits
"New"
Configurable with n bits
"Old 1"
"Old 2"
"Old 3"
"Old 1"
"Old 2"
"Old 3"
"new" way = compatible with other schemes
"old" way = incompatible with other schemes
PRIOR ART

Fig. 2

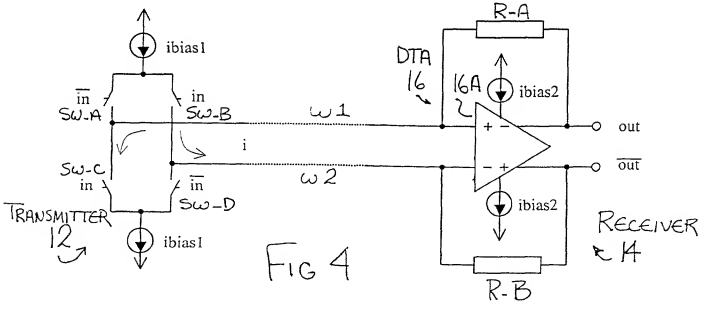
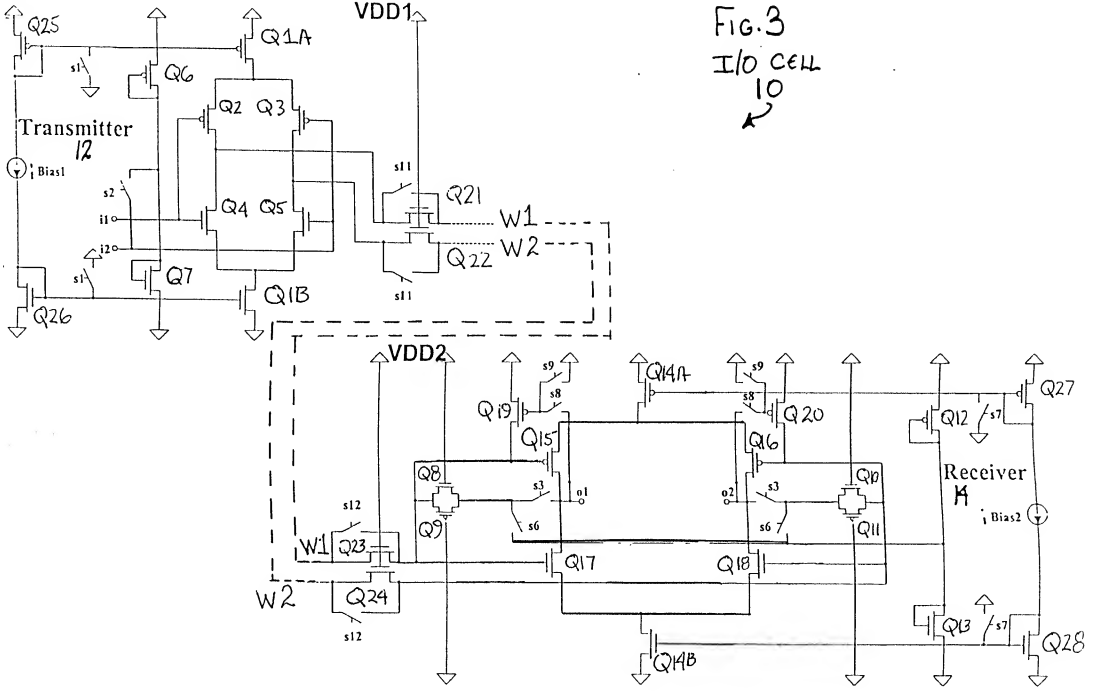

ibias1
R-A
DTA
16
16A
ibias2
in
SW-A
SW-B
ω1
out
i
SW-C
SW-D
ω2
TRANSMITTER
12
ibias1
ibias2
RECEIVER
14
R-B
in
out

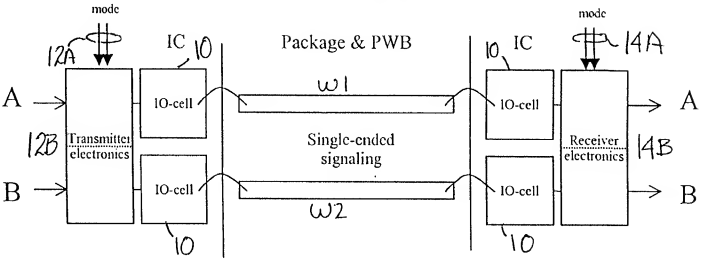
FIG 4


VDD1
VDD2
Transmitter
12
Receiver
14
I/O CELL
10
Q25
Q1A
Q6
Q2
Q3
Q4
Q5
Q7
Q1B
Q26
Q21
Q22
W1
W2
Bias1
Bias2
s1
s2
s3
s6
s7
s8
s9
s11
s12
i1
i2
o1
o2
Q19
Q15
Q8
Q9
Q23
Q24
Q17
Q14A
Q14B
Q20
Q16
Q10
Q11
Q18
Q12
Q13
Q27
Q28

Two single-ended links:
(current or voltage mode)

Modes 1, 2, 3, 4

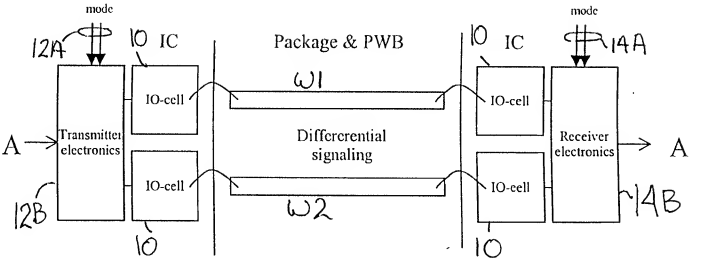
FIG. 5A



Single differential link:
(current or voltage mode)

Modes 5, 6, 7, 8

FIG. 5B



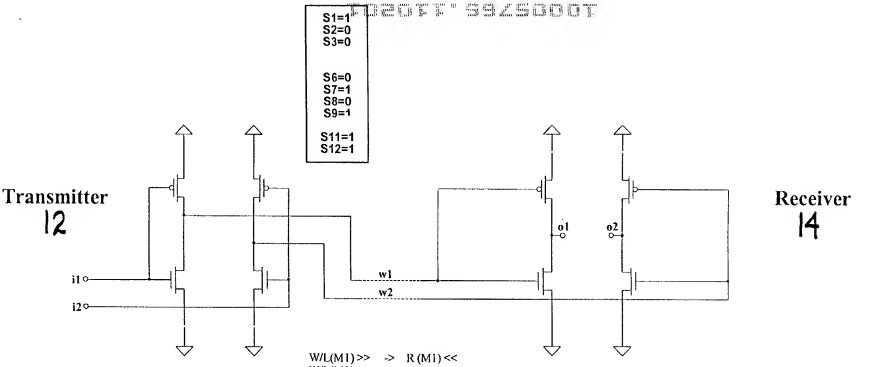

S1=1
S2=0
S3=0
S6=0
S7=1
S8=0
S9=1
S11=1
S12=1
Transmitter
12
Receiver
14
i1
i2
w1
w2
o1
o2
W/L(M1)>> -> R(M1)<<
W/L(M2)>> -> R(M2)<<
W/L(M3)>> -> R(M3)<<
W/L(M4)>> -> R(M4)<<

Fig. 6

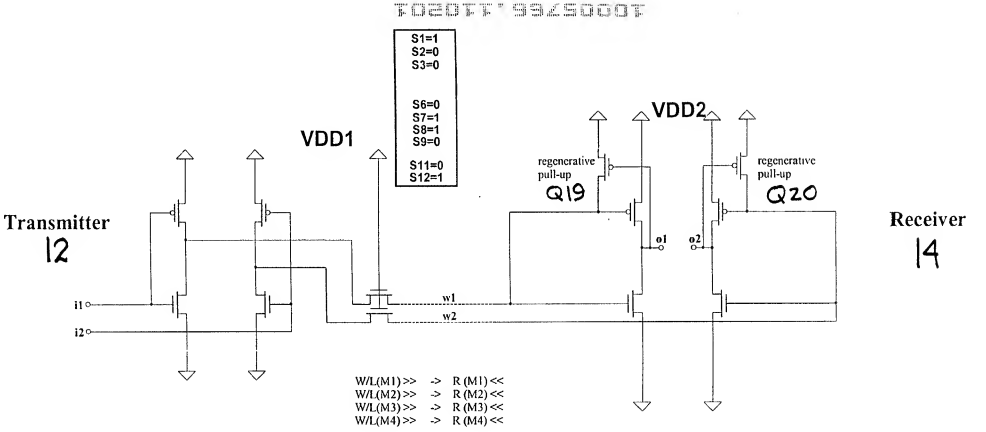

S1=1
S2=0
S3=0
S6=0
S7=1
S8=1
S9=0
S11=0
S12=1
VDD1
VDD2
regenerative pull-up
Q19
regenerative pull-up
Q20
Transmitter
12
Receiver
14
i1
i2
w1
w2
o1
o2
W/L(M1)>> -> R(M1)<<
W/L(M2)>> -> R(M2)<<
W/L(M3)>> -> R(M3)<<
W/L(M4)>> -> R(M4)<<

Fig. 7

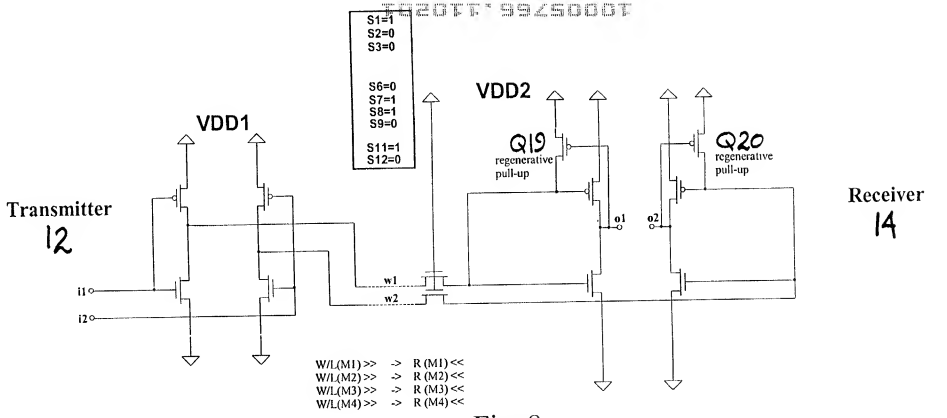

S1=1
S2=0
S3=0
S6=0
S7=1
S8=1
S9=0
S11=1
S12=0
VDD1
VDD2
Q19
regenerative
pull-up
Q20
regenerative
pull-up
Transmitter
12
Receiver
14
i1
i2
w1
w2
o1
o2
W/L(M1)>> -> R(M1)<<
W/L(M2)>> -> R(M2)<<
W/L(M3)>> -> R(M3)<<
W/L(M4)>> -> R(M4)<<

Fig. 8

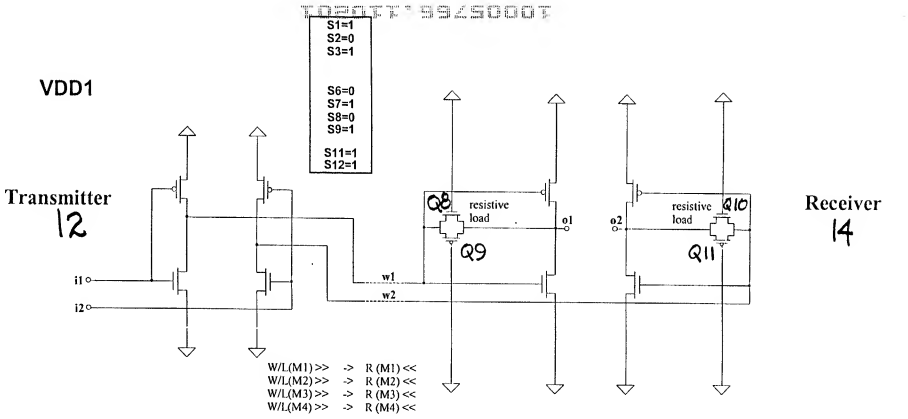

S1=1
S2=0
S3=1
S6=0
S7=1
S8=0
S9=1
S11=1
S12=1
VDD1
Transmitter
12
Receiver
14
Q8
resistive
load
Q9
Q10
resistive
load
Q11
o1
o2
i1
i2
w1
w2
W/L(M1) >> -> R (M1) <<
W/L(M2) >> -> R (M2) <<
W/L(M3) >> -> R (M3) <<
W/L(M4) >> -> R (M4) <<

Fig. 9

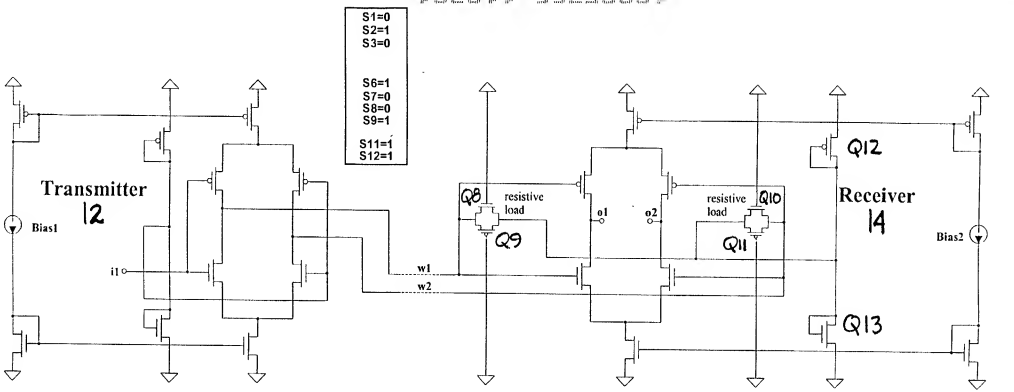

S1=0
S2=1
S3=0
S6=1
S7=0
S8=0
S9=1
S11=1
S12=1
Transmitter
12
Bias1
i1
w1
w2
Q8
resistive
load
Q9
o1
o2
resistive
load
Q10
Q11
Q12
Receiver
14
Bias2
Q13

Fig. 10

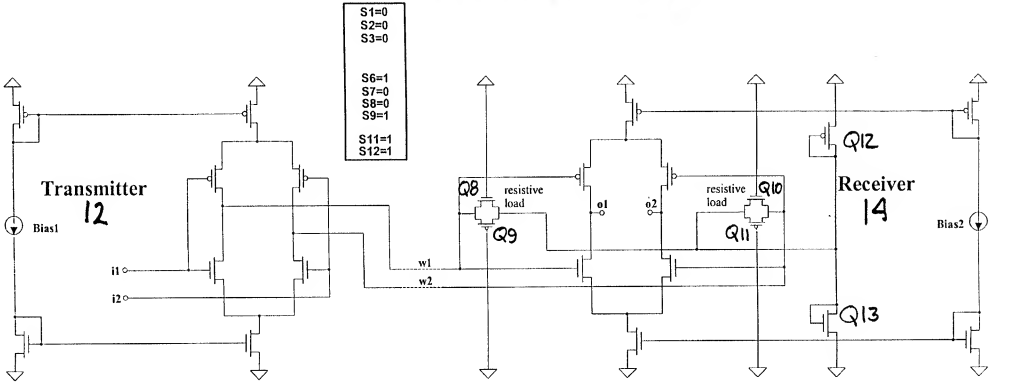

S1=0
S2=0
S3=0
S6=1
S7=0
S8=0
S9=1
S11=1
S12=1
Transmitter
12
Bias1
i1
i2
w1
w2
Q8
resistive
load
Q9
o1
o2
resistive
load
Q10
Q11
Q12
Receiver
14
Bias2
Q13

Fig. 11

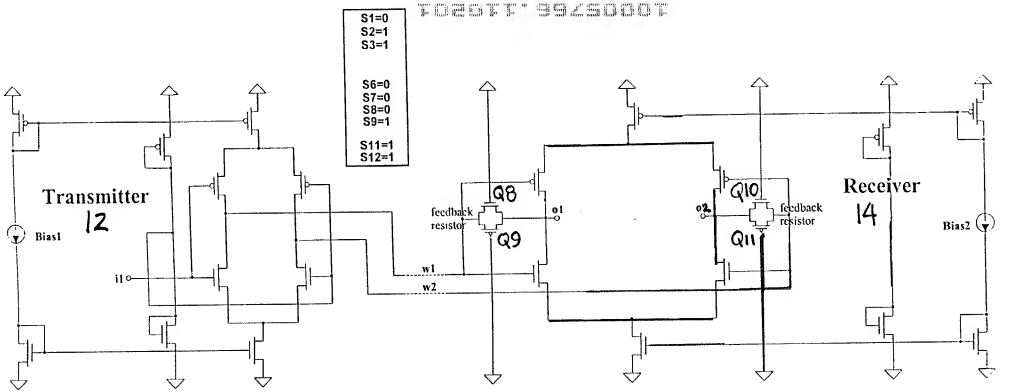

S1=0
S2=1
S3=1
S6=0
S7=0
S8=0
S9=1
S11=1
S12=1
Transmitter
12
Bias1
i1
w1
w2
Q8
Q9
feedback
resistor
o1
Q10
Q11
o2
feedback
resistor
Receiver
14
Bias2

Fig. 12

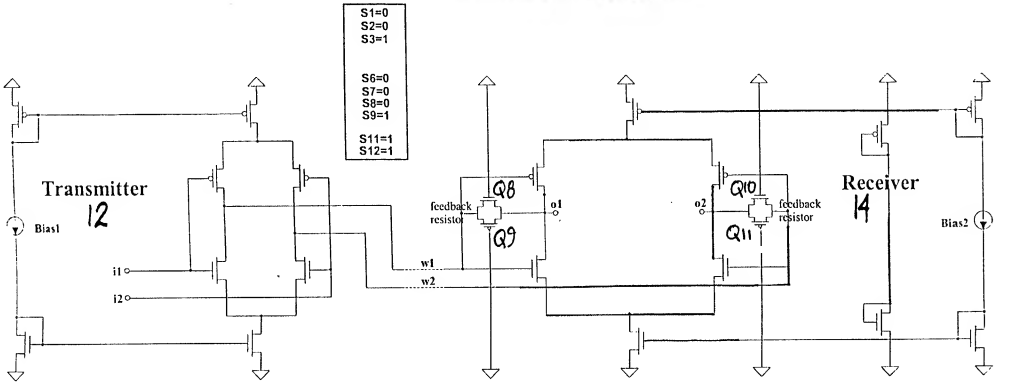

S1=0
S2=0
S3=1
S6=0
S7=0
S8=0
S9=1
S11=1
S12=1
Transmitter
12
Bias1
i1
i2
w1
w2
feedback resistor
Q8
Q9
o1
o2
Q10
Q11
feedback resistor
Receiver
14
Bias2

Fig. 13

Receiver:	Transmitter:
S4=1 S5=0 S10=0 S13=0 S14=0 S15=1 S16=0	S4=0 S5=1 S10=1 S13=0 or 1, equal to S11 S14=1 S15=0 S16=0 or 1, equal to S2

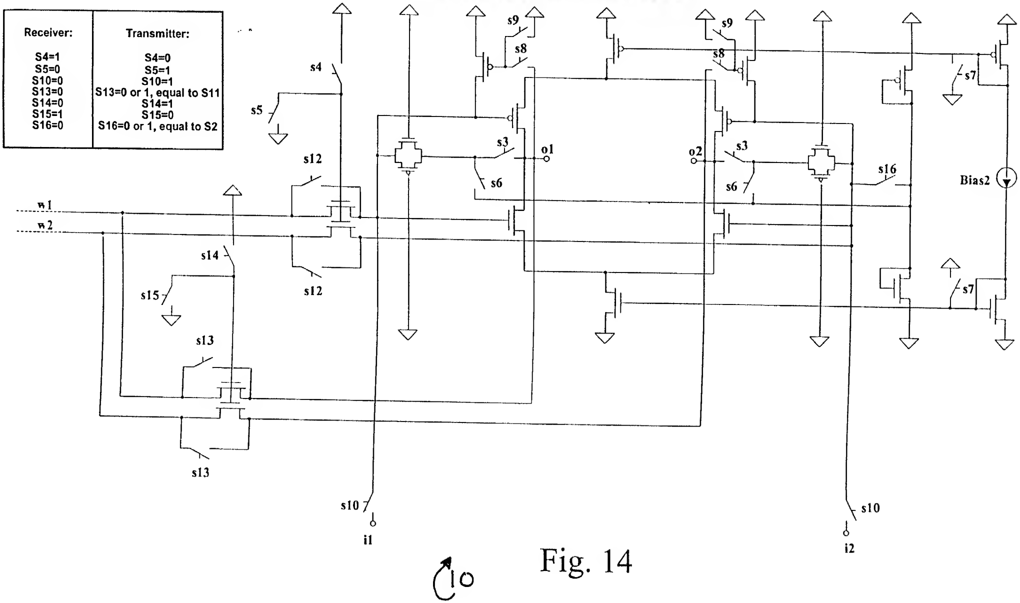


Fig. 14